GaN PROTOTYPE ACCELERATOR

Industry Day

June 19th, 2025

David Via
MMEC

Rehan Kapadia
CA DREAMS
MOSIS 2.0

Paul Colestock
MMEC

Mike Barsky
Northrop Grumman
Microelectronics Center

https://ganchallenge.com

Agenda

- GaN Prototype Accelerator overview – David Via (MMEC) 10 min
- GaN15 PDK and technology offering – Mike Barsky (NGC) 15 min
- MOSIS 2.0 model – Rehan Kapadia (CA DREAMS) 15 min
- EDA tool access – Paul Colestock (MMEC) 15 min
- White Paper Application process – David Via (MMEC) 15 min
    - White paper criteria
    - Quad
    - Timeline
- Wrap Up / Q&A – All 20 min

GaN PROTOTYPE ACCELERATOR

Overview

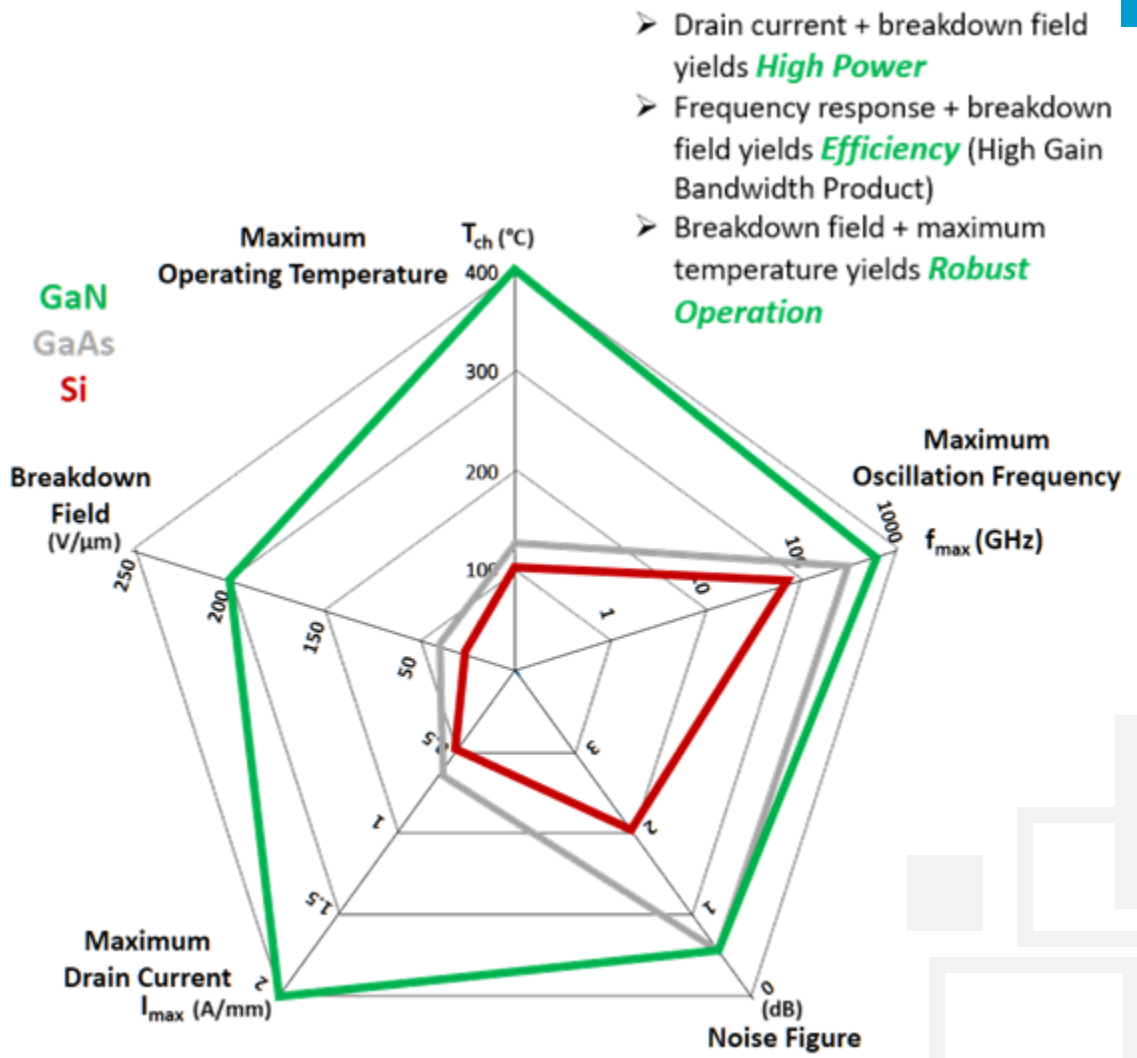
David Via

Director of Programs

MMEC

Why GaN?

- Performance advantages for RADAR, EW, and Communications systems critical for US military superiority and dual use RF applications
- 5x -10x increase in RF power over competing technologies
- Superior power coupled with frequency response enables high efficiency broadband circuit solutions
- Combination of material parameters results in reduced C-SWAP
- Capitalize on over $0.5B DoD investment in domestic GaN development and maturation



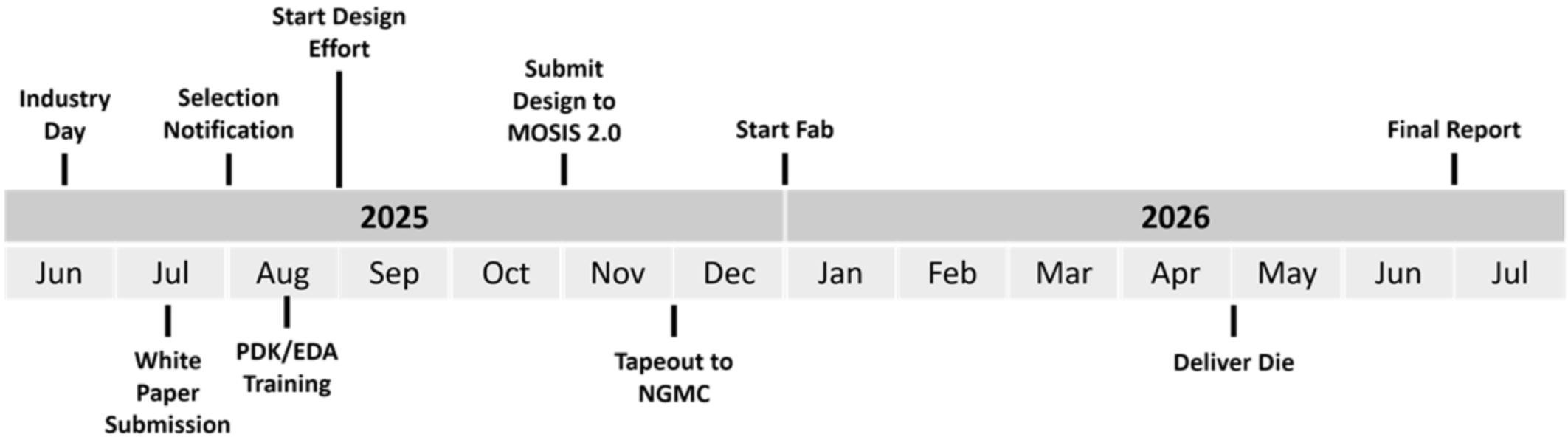
GaN Prototype Accelerator Overview

- The CA DREAMS and MMEC Hubs of the Microelectronics Commons program are announcing a GaN Prototype Accelerator Multi-Project Wafer (GaNPA MPW) Opportunity
- For this initial Opportunity, CA DREAMS and MMEC are partnering with the Northrop Grumman Microelectronics Center for access to their GaN15 PDK
- GaNPA Objectives:
  - Lower barriers to entry to advanced GaN technology
  - Engage with non-traditional GaN power amplifier designers
  - Foster domestic design and fabrication capability
  - Enable rigorous RF design practices
  - Provide solutions for the benefit of National Security
- Fee Structure:
  - $20K Large Business
  - $10K Small Business
  - $5K Academia

GaNPA Offering

- Design support services
- EDA tool access
- GaN15 test devices
- Die area on GaN15 MPW
  - MPW lot PCM data
- RF characterization support

Timeline



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GaN
PROTOTYPE ACCELERATOR

GaN15 PDK Technology Offering

Mike Barsky

Director, General Manager

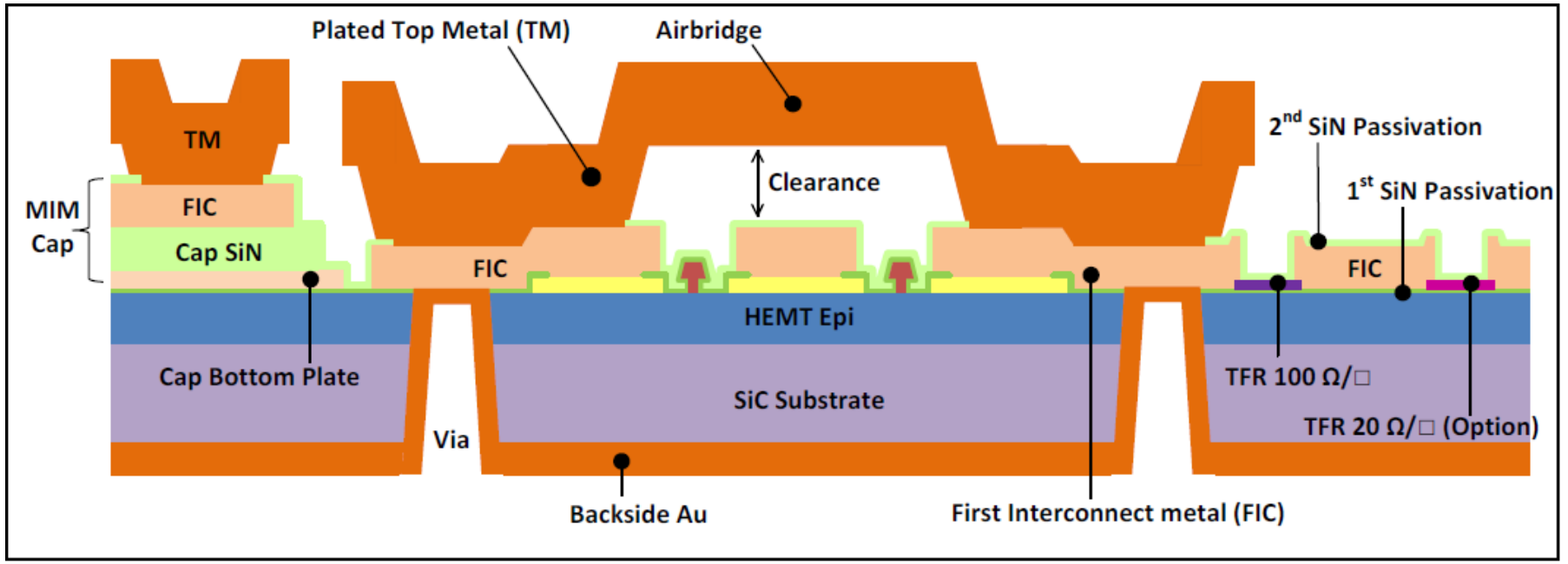
Microelectronics Products and Services Business Unit

Northrop Grumman

Northrop Grumman Microelectronics Center (NGMC) Space Park Foundry (SPF) GAN15PWR Description

- NG Space Park Foundry GAN15PWR technology is at TRL9/MRL9 and supports high frequency terrestrial applications
  - 0.15um gate length
  - MIM Capacitor: 300 pF/mm^2 MIM capacitor
  - Thin Film Resistor (TFR): two values are available: 20 ohm/sq and 100 ohm/sq TFR (both can be used)
  - Substrate thickness: 3mil Silicon Carbide (SiC) with thru-substrate-via
- 40GHz load-pull evaluation measures 5W/mm power density and >8dB associated gain at the peak Power Added Efficiency (PAE) > 40%

NGMC GaN15 Technology MMIC Stack-Up Diagram



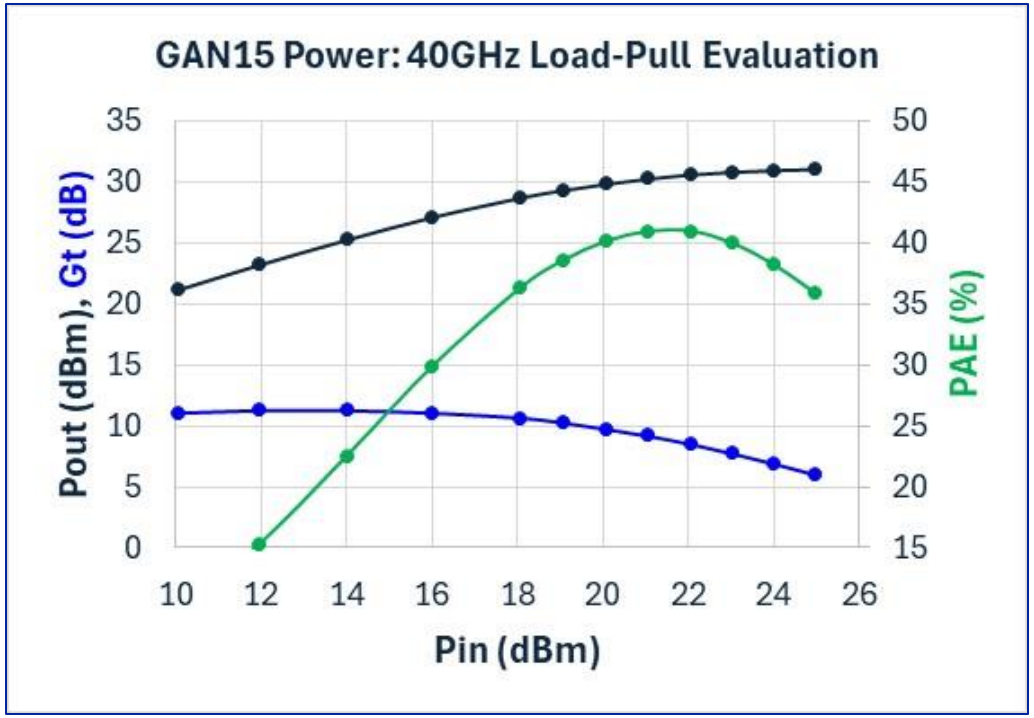
NGMC SPACE PARK FOUNDRY
GAN15PWR Description

NORTHROP GRUMMAN

NGMC GaN15 HEMT Device Performance

Parameter		Unit of Measure	GAN15 POWER
Max. Operation Voltage		V	28
Recommended Max. Frequency		GHz	80
DC	I_{max}	mA/mm	1350
	G_{mpeak}	mS/mm	410
	3-terminal Vbr	V	140
Small Signal	F_t	GHz	79
	F_{max}	GHz	163
10GHz CW Loadpull	P_{out}	W/mm	5.5
	PAE	%	49
	Gain @ peak PAE	dB	14.8
40GHz CW Loadpull	P_{out}	W/mm	4.1
	PAE	%	41
	Gain @ peak PAE	dB	8.3
Noise	Nfmin @ 30GHz	dB	1.5

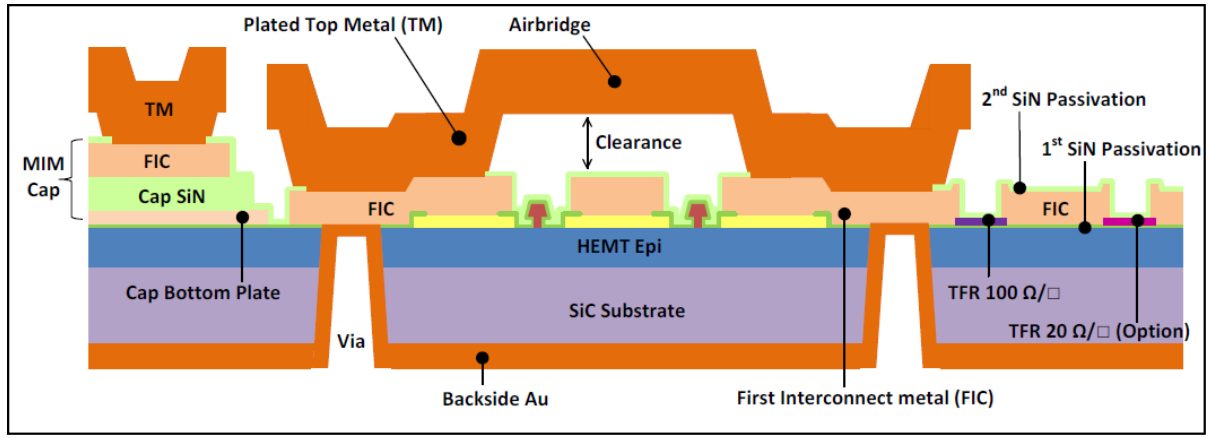
Assessment based on 4-Finger 200um coplanar device



NGMC SPACE PARK FOUNDRY
GAN15PWR Description

GaN15PWR Passive Components

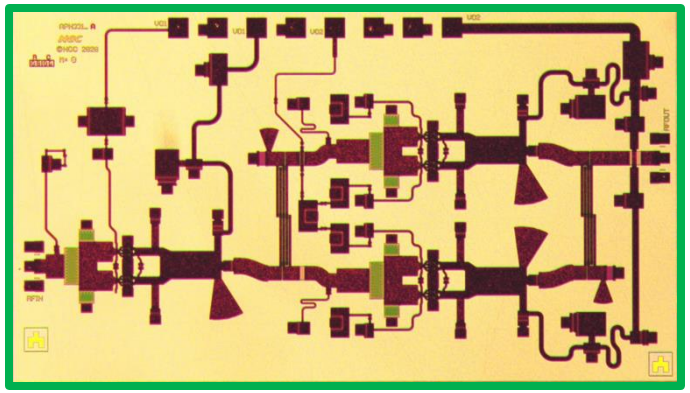
Component	Parameter	Unit	Min	Typical	Max
MIMCAP	Sheet Capacitance	pF/mm^2	270	300	330
MIMCAP	Max. Op. DC Voltage	V			28
TFR20	Sheet Resistance	Ohm/sq	85	100	115
TFR100	Sheet Resistance	Ohm/sq	17	20	23
First-InterConnect (FIC) Metal	Sheet Resistance	Ohm/sq	0.023	0.0315	0.04
Top Metal	Sheet Resistance	Ohm/sq	0.004	0.0065	0.009



GaN15PWR Design Example

- APN331, two stage high power amplifier using GAN15PWR technology
  - ➢ 2W output power

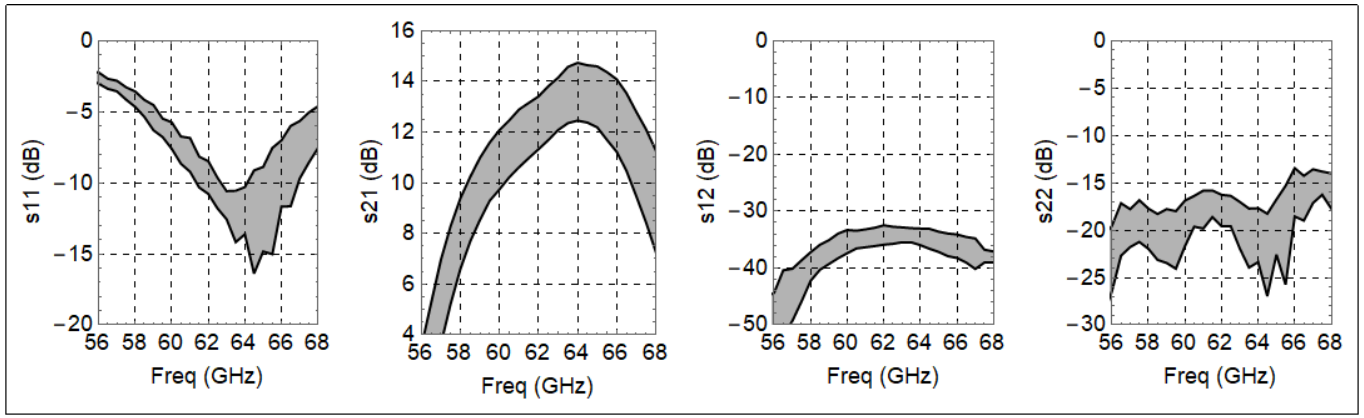
APN331 Optical Image

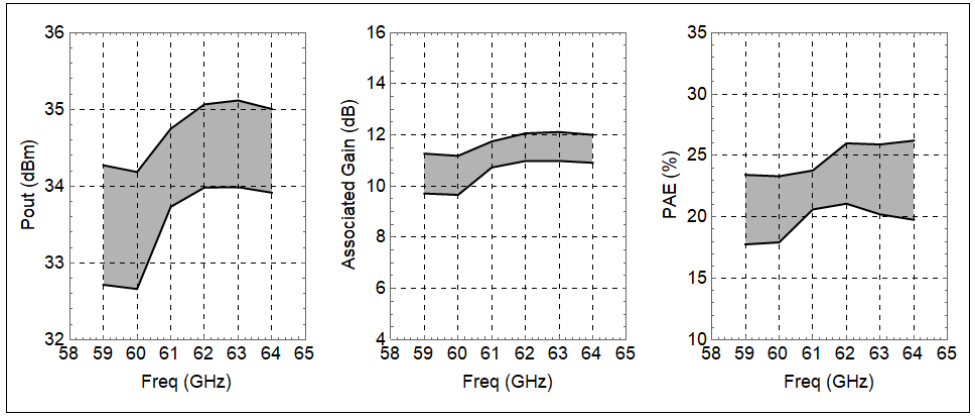


Chip size = 3.46 x 1.97 mm²

- **Performance Highlights**
  - – > 11dB s21 from 59GHz to 66GHz, 7GHz bandwidth
  - – 33dBm Pout with 10dB power gain and ~20% PAE across 4GHz from 60-64GHz
  - – Quiescent bias: 28V Vdq, 200mA/mm Idq

On-wafer CW s-par and pulse PiPO Frequency Response





10% to 90% Distribution - 1911 sites from 8 lots, 39 wafers

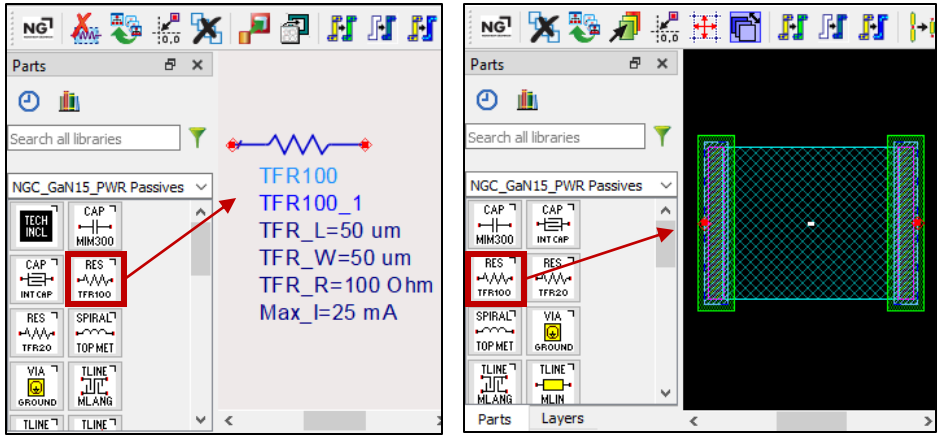
GAN15PWR demonstrates V-band manufacturability for superior performance/uniformity

GaN15PWR Process Design Kit

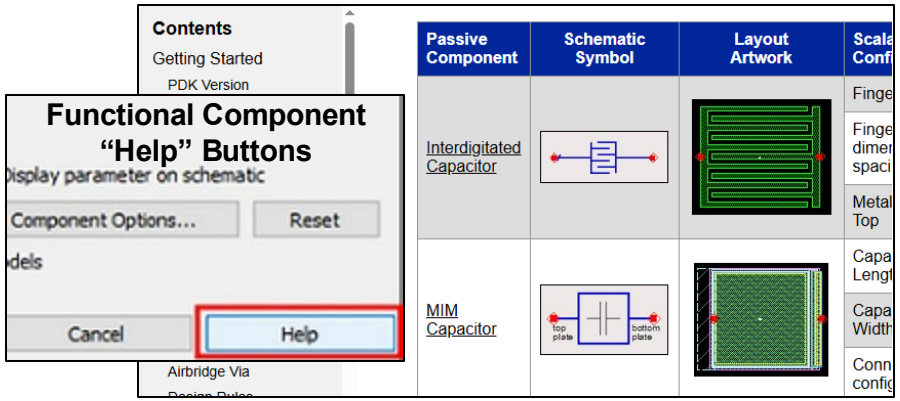
- Platform and environment
  - Keysight® ADS™ 2022u1 or newer required, 2023+ recommended *
  - Windows™ and Linux™ operating systems both supported

  * AWR™ PDK also available, but design verification and tapeout from ADS™ is preferred
- Schematic symbols include models
  - Active devices include scalable linear & non-linear models
  - Passives & transmission line models account for parasitics
  - Models support statistical analysis of process variability (ADS™ only)

Synchronized Schematic Symbols & Layout Artwork



Integrated HTML Based ADS™ PDK Manual



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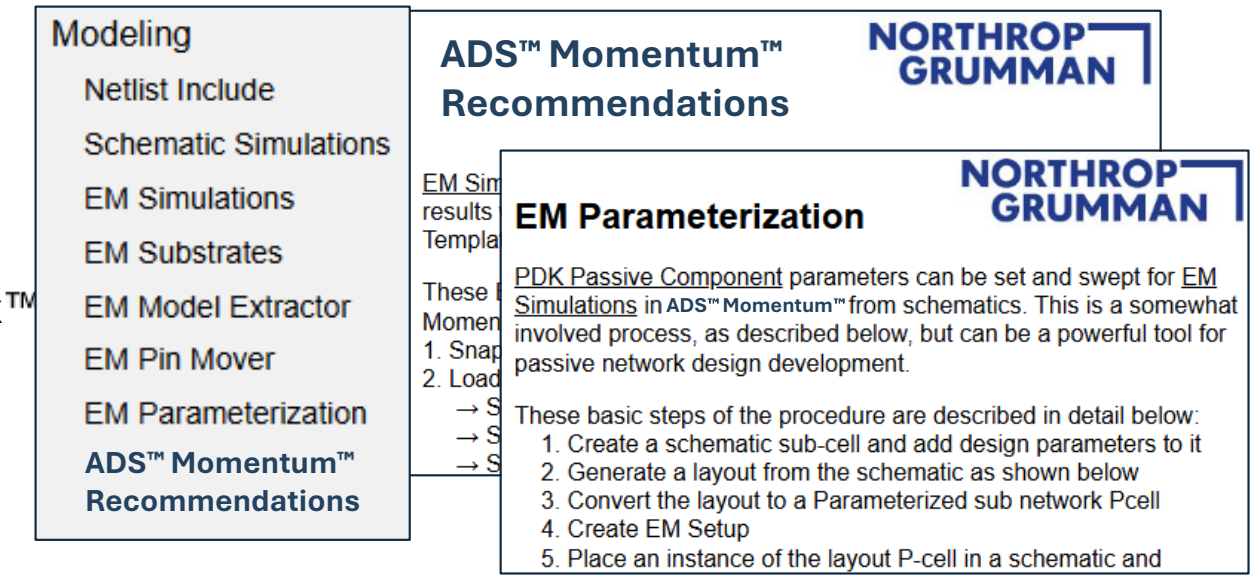
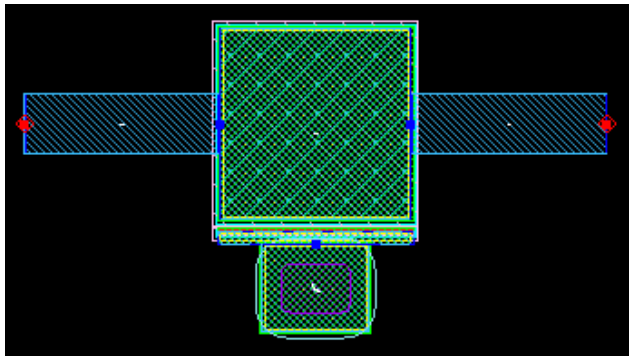
GaN15 PWR Process Design Kit

- Automated electro-magnetic simulation functionality
  - Layouts map into EM solvers automatically
  - ADS™ PDK includes an HFSS™ model extraction utility
- Full design verification functionality
  - ADS™ DRC and LVS
  - Assura™ DRC identical to foundry DRC (ADS™ in Linux™
- Custom ADS™ PDK utility functions
  - Reticle layout utility
  - Design tapeout utility
- Introductory PDK training can be made available

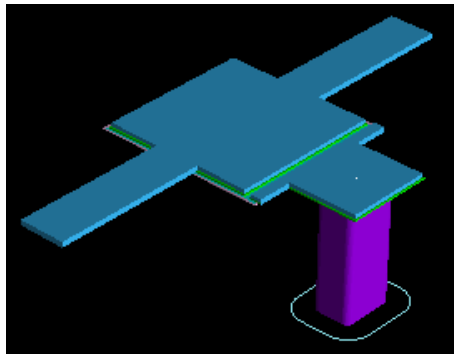
ADS™ PDK Manual Pages on Modeling



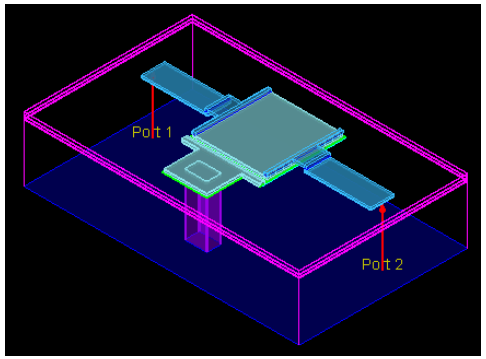
Layout 2D View



Layout 3D View



Extracted EM Model



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Assura and AWR are trademarks of Cadence®, Linux is a trademark of the Linux Foundation®

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MOSIS 2.0 Engagement Model

Prof. Rehan Kapadia

CA DREAMS / MOSIS 2.0

USC Information Sciences Institute

MOSIS 2.0 Open for Business

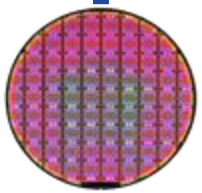
MOSIS 2.0 Workflow - GaN PA

System Brassboard

Packaging & Test

Design A	Design B	Design C
ADVANCED PACKAGING AND TEST	ADVANCED PACKAGING AND TEST	ADVANCED PACKAGING AND TEST

- Enable backend process capabilities
- Offer post-MPW testing & characterization



MPW Wafer

Request for Design Proposals from

- Private
- Start-up
- University
- Small Business

MMEC™ ACCELERATE : COLLABORATE : EXECUTE

DREAMS Defense Ready Electronics and Microdevices Superhub

MOSIS 2.0

Proposal Review

Project A	Project B
Project C	Project D

- Solicit Design Concept
- Provide Technical Guideline
- Conduct Mult-tiered Review
- Select Prototypes for MPWs
- Host Technical Q&A Session

.....

Prototype Integration and Engineering Service (PIES)

Design A | Design B | Design C | Design D

Quick Prototyping
Design Support
Data Management
IP/EDA Tools
MPW Accessibility

Cross-Hub Enablement

Superhub Cloud

IP	Manufacturability	Availability/Cost
EDA Tools Design IP Library PDK Library	Process Yield Process SPC/Cpk Validated Services	MPW Schedule Tool availability & Schedule

NORTHROP GRUMMAN

Foundry Services

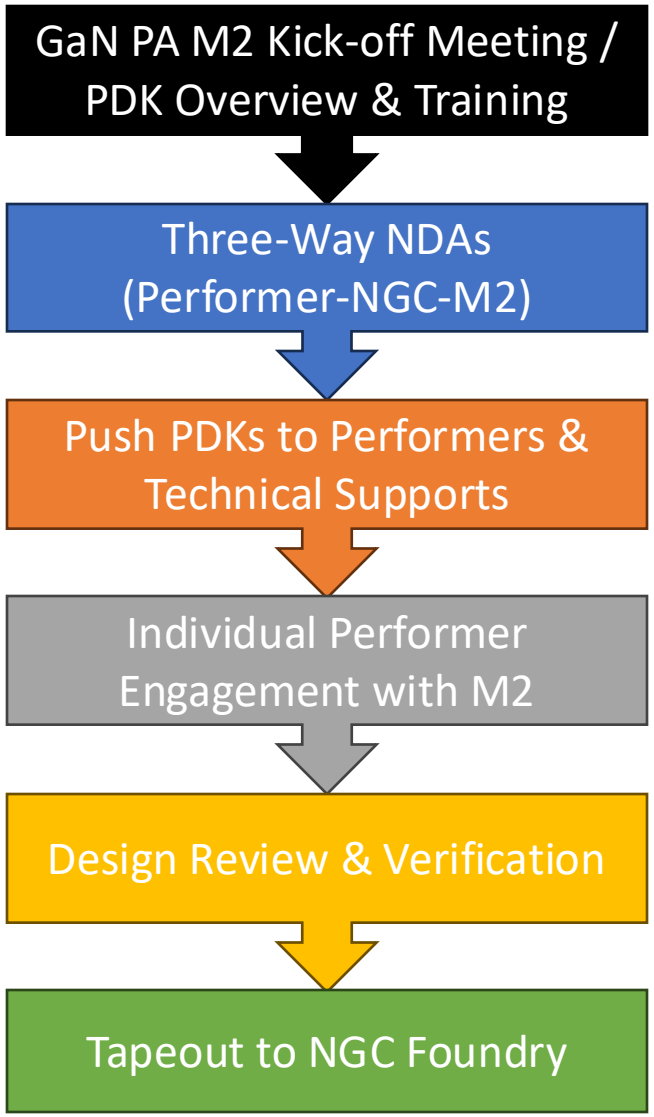
DOD-Volume Fabs

- NGC GaN15
- Packaging (Optional)
- Dicing (Optional)

Development Flow

Data Flow

MOSIS 2.0 Onboarding Procedure



- **Kick-off Meeting / PDK Overview & Training** – Officially launch the program, walk through the GaN15 MPW process, and provide tool-based training on the PDK and simulation environment.
- **Three-Way NDA** – Execute NDAs among each performer, NGC, and MOSIS 2.0 to enable secure sharing of PDKs and design files.
- **PDK Release** – Provide GaN15 PDK packages with setup instructions, design rules, symbol libraries, and simulation models for supported EDA tools.
- **Individual Performer Engagement** – Hold dedicated technical sessions with each performer to review design concepts, clarify foundry constraints, and answer detailed questions.
- **Iterative Design Review** – Conduct multiple rounds of design reviews to verify DRC/LVS compliance, guide improvements, and prepare designs for aggregation.
- **Tapeout to Foundry** – Finalize and aggregate all validated designs, then submit to NGC for MPW fabrication and subsequent die delivery.

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EDA Tool Access

Paul Colestock

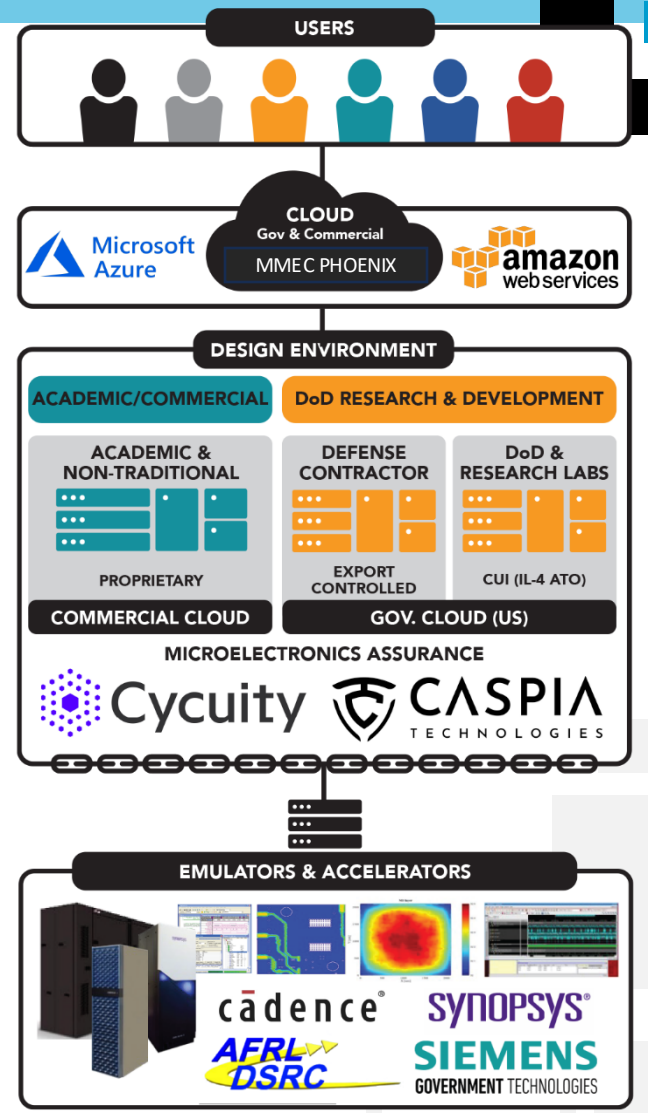
Director of Commercial Innovation

MMEC

GaN Prototype Accelerator - DESIGN & EDA

- Designers get access to MMECs hosted DESIGN framework
  - PDKs, EDA, Compute and Repository for data/final gds
- GaN15 has PDKs to support both ADS and AWR
  - Design Verification and tape-out from ADS is preferred
- ADS tools available: W3606B & W3050E
- ***NOTE: EDA tools only for use within US IP Domain***

Hosted ADS licenses are the W3606B & W3050E and Include	
ADS Core	ADS platform, schematic capture, data display, optimization, Python scripting automation & more.
EM Design Core	3D solid modeling environment. Does not include EM simulators.
Layout	3D physical design, routing, verification (LVS, DRC, LVL, ERC) & industry standards file import/export environment.
RF Ckt Sim	Linear, harmonic balance, circuit envelope, and transient/ convolution circuit simulators.
RFPro	FEM and Momentum 3DEM simulators integrated in a powerful UI for automating EM-Circuit cosimulation.
Electrothermal Sim	Electro-Thermal Simulator for optimal circuit simulation accuracy by accounting for electrothermal heating.



GaNPA: EDA Tool User Onboarding

- Once users have completed requisite NDAs and EULAs, users will get an onboarding email and a link to log into the DESIGN environment. User-name and temp password will be provided as well as an email address for login support.
- Once users log in and change their password, they will see a desktop and side-bar menu item with options to get help, access documentation, launch the ADS environment, and to submit their gds and associated documents to MOSIS2.0.
- All user working directories and environment paths to PDKs are preconfigured.
- Users can start their design in the ADS platform and launch any necessary tools from within the platform (EM, Electro-thermal, DRC, LVS etc).
- All associated user documentation and training materials can also be accessed through the EDA platform directly as part of the GAN15 PDK integration.

NOTE: Design activity is expected to be performed on provided cloud compute resources

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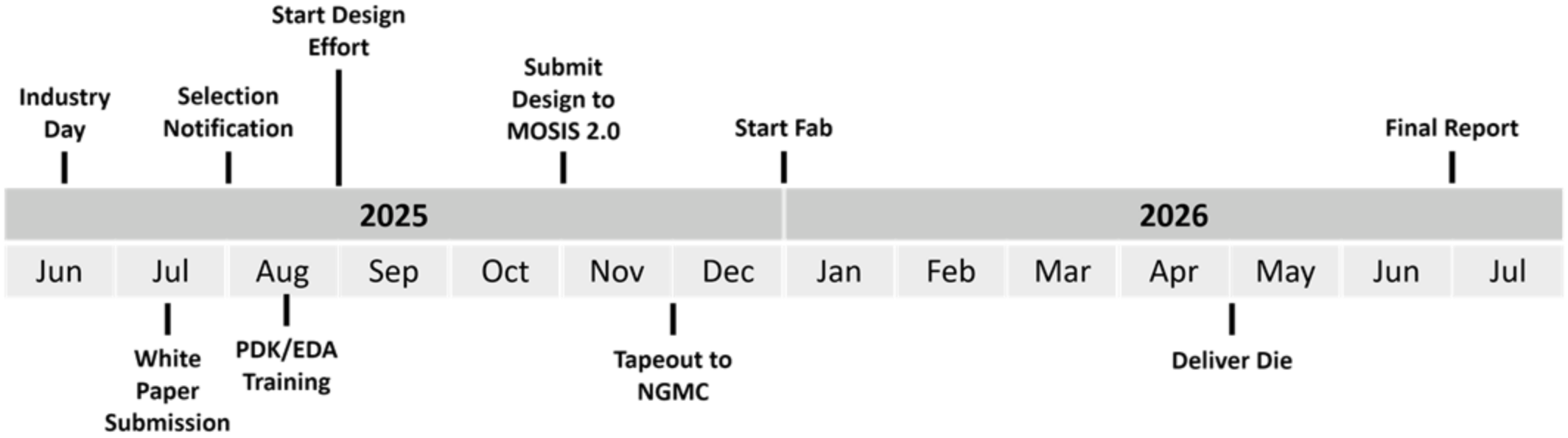
White Paper Submission

David Via

Timeline



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White Paper

- White Paper submission deadline is **July18th, 2025 –** https://ganchallenge.com
- Content
  - Application – Clearly describe application or application area being targeted, circuit design concept, and how proposed design concept will provide novel or unique solution enabled by advanced GaN technology offering and/or innovative design approach
  - Performance Metrics – Identify performance objectives and how these improve on state-of-the-art discussing how proposed application is addressed today and what are the limits of the current approach
  - Experience – Discuss prior experience does team have with circuit design, EDA tool use, GaN technology, and RF testing/characterization
  - Transition & Impact – Discuss potential technology transition opportunities or strategies, market relevance, and potential for reuse/modification of GaN design
  - Die Area and EDA Tools – Identify what die area and EDA tools are being requested – declare number of intended users (team roster)
- 5-page limit for technical submission
- Quad (template provided)

Required Quad

DREAMS Defense Ready Electronics and Microdevices Superhub | MMEC ACCELERATE : COLLABORATE : EXECUTE | NORTHROP GRUMMAN

Project Title

Lead Organization / PI / contact information

Team Logos

Innovative Claims

- What is the problem? Why is the solution challenging?
- How is it done today, and what are the limits of current practice?
- What is unique about your approach? Why will it succeed?
- Include a graphic that summarizes the proposed effort if supportive

Technical Area and Impact

- What application area does this proposal address?
- What are the proposed circuit performance objectives (metrics)?

- What is the potential impact of the proposed effort? Who Cares?
- What is potential technology transition strategy? Identify transition partners within DoD and/or commercial industry, if possible

Technical Rationale, Risks, and Requirements

- What enabling/supporting technology, if any, is needed for the proposed approach?
- What are the technical risks and how do you plan to address them?
- Identify die area being requested (6mm x 4mm, 4mm x 4mm, or 5mm x 5mm)
- Identify required EDA tools and number of intended users (team roster)
- Describe RF characterization capabilities (in house, outsourced, other, …)

Team Organization

- Business sector – large business, small business, academia, government
- Proposed team organization and rolls/responsibilities

White Paper Evaluation Criteria

- Technical Merit (20%) – What technical challenge and application area is being addressed? How is proposed circuit concept and/or GaN15 technology offering providing novel or unique solution?
- Metrics (20%) – Proposed circuit concept performance objectives. How do these improve on SOTA? What are the limitations of current approaches?
- Desired Outcomes (35%) – Circuit design technology transition strategy identifying end users within DoD and/or commercial industry (if possible), journal/proceedings publication(s), thesis/dissertation research, …
- Design and Test Capability (25%) – Relevant design capability of team referencing prior GaN or other circuit design experience, familiarity with EDA tools, and proposed electrical characterization plan/methodology
- Die Area and EDA request – Die area being requested (6mm x 4mm, 5mm x 5mm, or 4mm x 4mm), EDA tools and number of licenses that are being requested
- Business Sector – large business, small business, academia, government
- Quad (template provided)

Summary Report

- Executive Summary
  - Concise overview of design project highlighting technology application and performance goals
- Circuit Description
  - Recap of circuit concept noting any variation from original concept
- Test Results
  - Measured data versus circuit design simulation of Key Performance Parameters (KPPs)
  - Analysis of performance deltas
- Lessons Learned
  - Experience working with CA DREAMS, MOSIS 2.0, MMEC, EDA tools, GaN15 PDK, …
- Recommendations
  - Suggestions to improve future GaNPA MPWs
  - Identify other foundries and technologies of interest for future MPWs

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Q&A

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Backup

Test Support

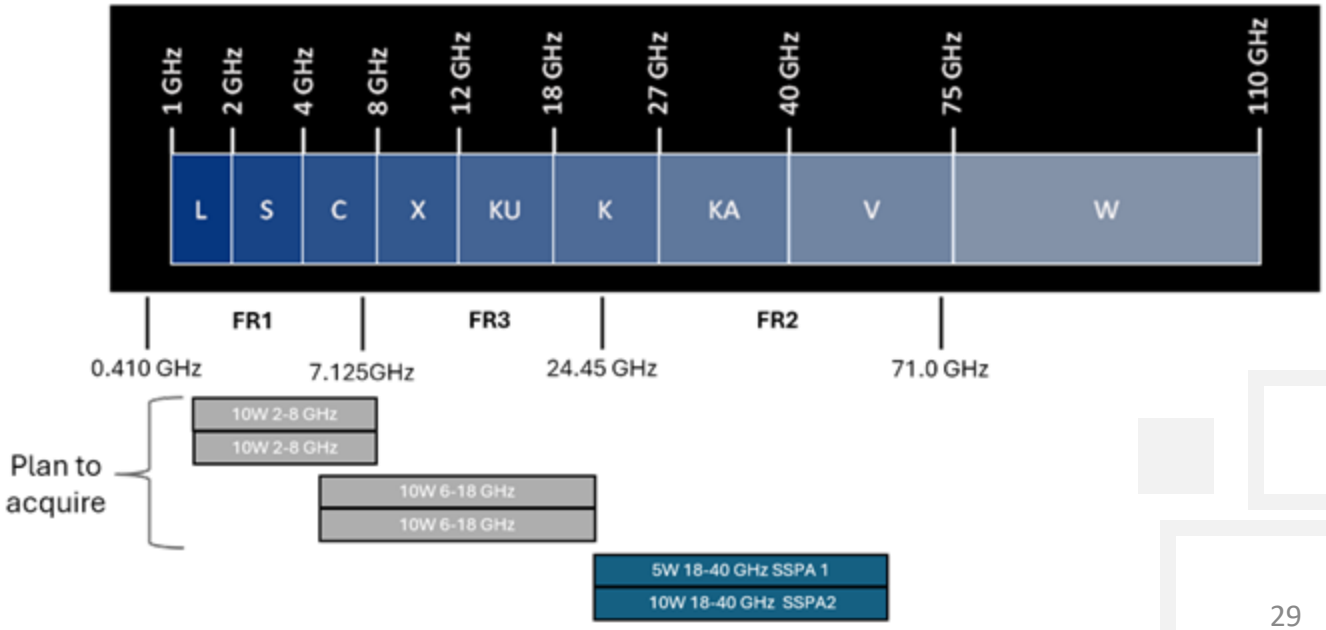
- RF Characterization services available via MMEC at The Ohio State University

Current Capabilities:

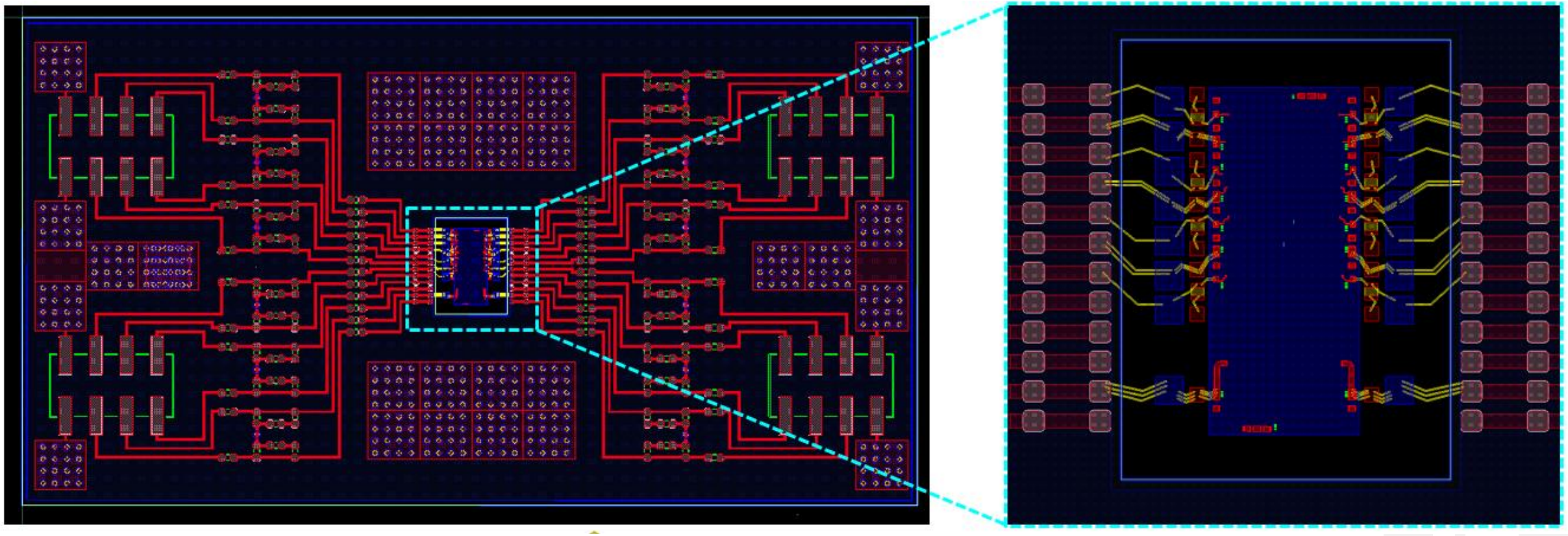
- Maury MT2000
- RF small signal up to 67 GHz
- Ka-band load pull (18-40 GHz)
- Pulsed s-parameters and load pull
- -30C to 300C temp stage
- AMCAD Pulsed IV

Future Capabilities:

- Additional SSPAs to support load pull at FR1, FR3, and FR2 or S-band thru Ka-band
- (2) 2-18 GHz
- (2) 6-18 GHz
- Enable harmonic load pull



RF Flex Test Board



- Low- cost solution for circuit stabilization
- Power In / Power Out (PIPO) circuit evaluation